Design Techniques to combat Process, Temperature and Supply variations in Bluetooth RFIC.

Y. Theng Tee, Y. Hwa Seng, L. Poh Boon, T. Kwang Hung, S. Tachi, K. Soo Ling, T. Murakami, S. Jin Hui, L. Choon Tiong, T. Lin Choon, W. Wing Kheng, X. Qi Jun, L. Chiao Meng, L. Shio Hwi, X. Wei, M. Itoh

RFIC Development & Design Department, OKI Techno Centre (Singapore) Pte Ltd, Teletech Park, Singapore Science Park II, Singapore 117674

Abstract — **A fully integrated Bluetooth RF transceiver with sensitivity up to –85 dBm with ±2 dB process variation has been achieved. The sensitivity only varies ±1 dB from 2.7 to 3.3V and ±1.5 dB from –40 to +90°C. This RFIC is fabricated using a 0.35µm CMOS process and can withstand a maximum input power of +5 dBm for 0.1 % BER.**

I. Introduction

The low cost and high level of integration makes CMOS process a popular choice for implementation of RFICs for Bluetooth applications [1]. However, one of the main challenges today is to achieve a high sensitivity across process, temperature and supply variations. This RFIC is designed to tackle this issue by means of compensation circuits introduced in both the RF and IF chains.

II. ARCHITECTURE AND DESIGN

Figure 1 shows the functional block diagram and chip micrograph of the RF transceiver. The receiver chain consists of a temperature compensated LNA and MIXER which generate quadrature IF outputs. The IF signals are then filtered by a complex bandpass filter which is auto-tuned by a gmc PLL to counter all process, temperature and supply variations. A simple two step control hysterisis AGC is placed before the ADC to further improve the system dynamic range by about 4~5 dB. The AGC output is sampled by an 8-bit low sampling rate (4 MHz) ADC for further digital processing. The digital processor will filter away any DC offset and residual interference in the signal before it is demodulated by a differential detector followed by a high speed dataslicer.

The transmitter chain begins with a digital gaussian pulse shaping circuit, followed by a temperature and channel compensated DAC which modulates a voltage controlled oscillator (VCO). The VCO output is then amplified by a power amplifier to attain the class 2 Bluetooth specification. A built in transmit/receive selector switch will channel the amplified signal to the BPF/antenna.

A. Receiver RF Architecture

Preceded by the duplexer (BPF and Switch), the low noise amplifier (LNA) and mixer serve as the RF front end of the receiver chain. Any variation in their gain and noise performance will affect the whole system's sensitivity. Therefore, the LNA and mixer have been designed to maintain a constant gain at all supply voltages (3V±10%) and temperatures (from -40°C to 90°C) by means of bandgap references and current compensation circuit to generate a positive predetermined current slope that is required by LNA and mixer. The purpose of the current compensation circuit is to compensate the variation of transistor gm over temperature for both circuits.

In the Gilbert Cell Mixer (GCM), an active load together with a Common Mode Feedback (CMFB) circuit is used. The CMFB circuit provides the gate biasing for the active load. While using the above current biasing condition, the gain of the GCM degrades because the active load exhibits lower load impedance as the bias current increases. This problem can be resolved by incorporating a current bypassing circuit into the mixer core. The current bypassing circuit directs portion of the current into the RF input transistors, bypassing the commutating switches and the active load as shown in Figure 2. This results in a reasonable load impedance and gm for the design.

B. Receiver IF Architecture

Figure 3 shows the IF architecture of the receiver. It consists of a 5th order butterworth polyphase filter [2], auto-tuner, AGC, ADC and RSSI. The 5 pole Gm-C polyphase filter is centered at 1MHz with a bandwidth of 1.1MHz. With the help of a limiter and careful gain distribution of each pole, both blocker and strong in-band signals are controlled. In addition, a diode connected PMOS between the differential output of each pole helps

0-7803-7694-3/03/$17.00 © 2003 IEEE

to suppress distortion due to strong in-band signals. As a result of this gain distribution, a low sampling rate ADC is possible. The auto-tuner circuit tunes the response and gain of the complex filter across all process, supply voltages and temperatures. RSSI function is introduced by tapping the voltage levels in the first 3 poles. At the output of the complex filter, a simple 2-step feed-forward AGC is introduced before the ADC. This helps to maintain a regulated input level to the ADC. The overall IF architecture provides a voltage gain of 24 or 36dB.

To combat the frequency offset inherent in GFSK design, the classical tracking method requires the fast tracking upon sync word detection period and quick switching to slow tracking upon payload detection which requires baseband intervention. This sudden switching also makes the design prone to noise and disturbance. To counter this problem, the data slicer is designed using digital signal processing to perform auto optimum tracking, which is tolerant to noise and transient disturbances. Digital slicing is performed through envelope detection, and is optimized to the Bluetooth modulation. It can handle frequency offsets of greater than ±150 KHz. This is done without the baseband intervention and results in good FER and BER. The digital demodulation employs a Nyquist FIR, whereby the I/Q is down-converted. The Nyquist FIR has a decimation rate of two fold with the even tap Nyquist FIR processing the I-rail samples only while the odd tap processes the Q-rail, with a speed reduction of half. This is followed by second order interpolation, demodulation and data slicing through threshold detection. Digital signal processing of the circuit is implemented through time-folding the operations and multi-domain clocking, hence achieving a better area performance.

C. *Transmitter Architecture*

In the transmitter chain, the frequency synthesizer is based on an integer-N architecture with implementation using open modulation techniques. The Digital Gaussian Low Pass Filter consists of a Digital Gaussian Pulse Shaping Block and a Digital to Analogue Converter (DAC) as shown in Figure 1. The main objective of the digital implementation of the GLPF is to eliminate any variations in signal amplitude due to process tolerances, temperature and supply changes. By using a bandgap voltage as a reference to the DAC, a supply-independent DC and AC output has been achieved for the GLPF output to maintain a consistent modulation index. To counter the effects of changes in modulation index due to temperature variations, a simple temperature compensation technique is implemented to provide a PTAT characteristic to the DAC output. A frequency compensation circuit is also implemented in the DAC to counter the modulation sensitivity change across different frequency channels.

III. MEASUREMENTS AND RESULTS

The IC is packaged in a 48-pin ball grid array (BGA). A total of 100 chips have been tested for their sensitivities for 0.1% BER. It is observed that the sample variations were –85dBm ± 2dB as shown in Figure 4. The combined effects of the various compensation techniques described above have yielded low sensitivity variations of ±1 dB from 2.7 to 3.3V and ±1.5 dB from –40 to +90°C as shown in Figure 5.

IV. CONCLUSION

The successful implementation of a fully integrated Bluetooth RF transceiver with sensitivity up to –85 dBm with ±2 dB process variation has been presented in this paper. This is achieved by means of various compensation techniques implemented in both the RF and IF chains. The sensitivity only varies ±1 dB from 2.7 to 3.3V and ±1.5 dB from –40 to +90°C. This RFIC is fabricated using a 0.35µm CMOS process and can withstand a maximum input power of +5 dBm for 0.1 % BER.

V. ACKNOWLEDGEMENT

The authors would also like to thank L. Wei Min, Z. Chuan Jun, C. Wei Khuen, L. Meng Xiong, Y. Chao for their dedicated support in realizing the completion of this paper.

REFERENCES

[1] Specifications of the Bluetooth System, Version 1.0B, December 1999

[2] J. Crols and M. Steyaert, CMOS Wireless Transceiver Design. Kluwer Academic Publishers, 1997

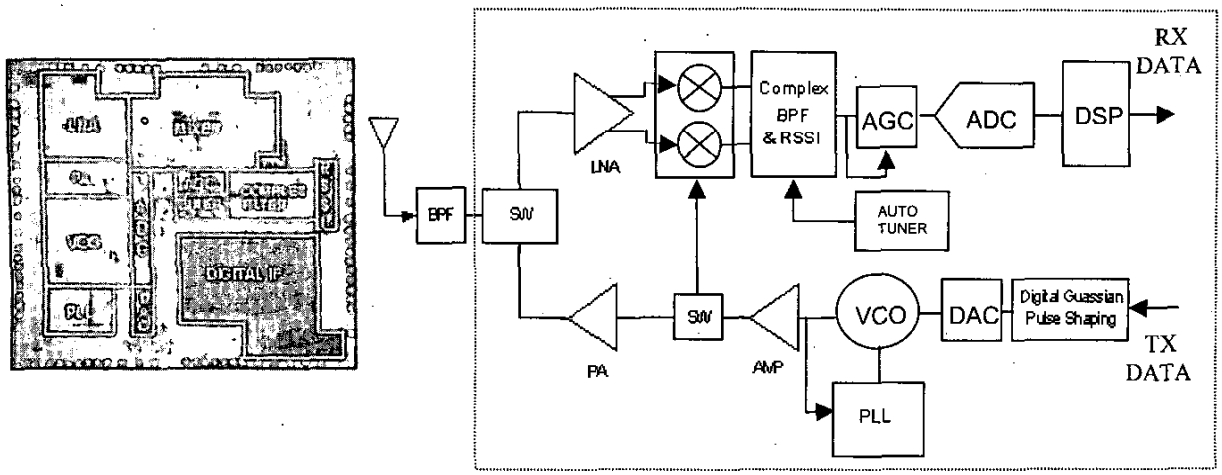

Fig. 1. Bluetooth Transceiver Micrograph and Block Diagram

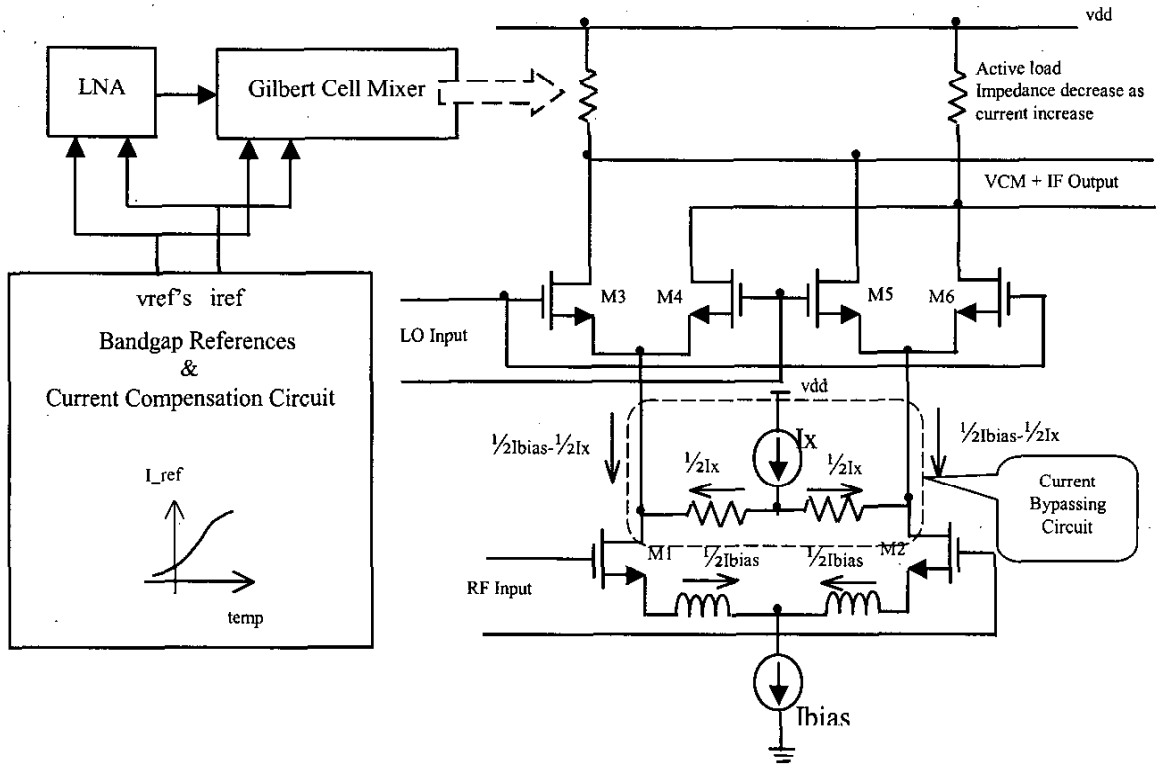

Fig. 2. Current Bypassing Circuit used in mixer

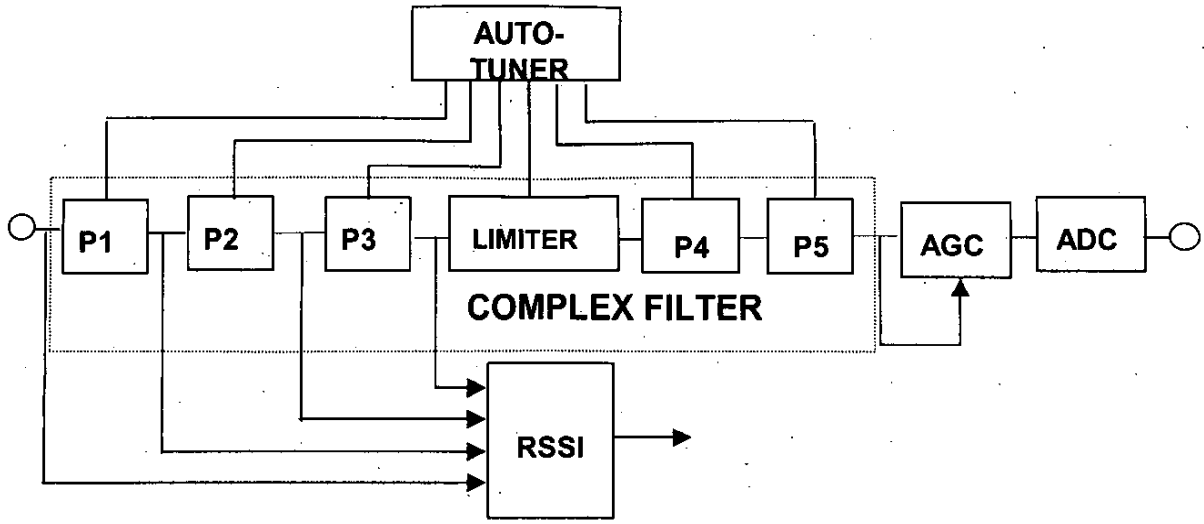

Fig. 3. Block Diagram of IF section

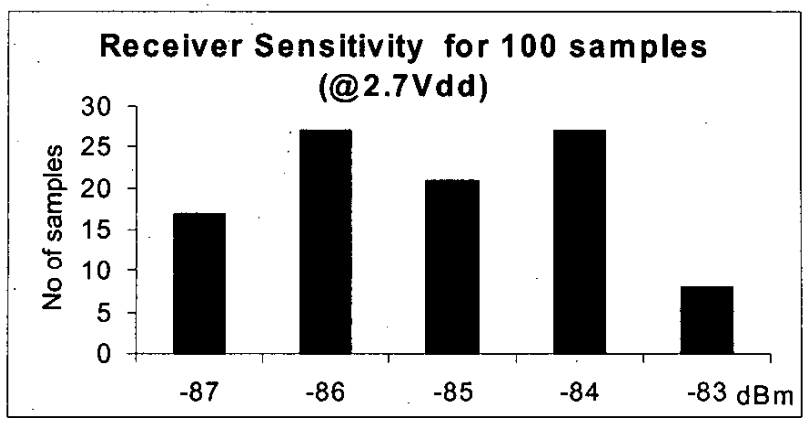

Fig. 4. Receiver Sensitivity Spread across 100 samples

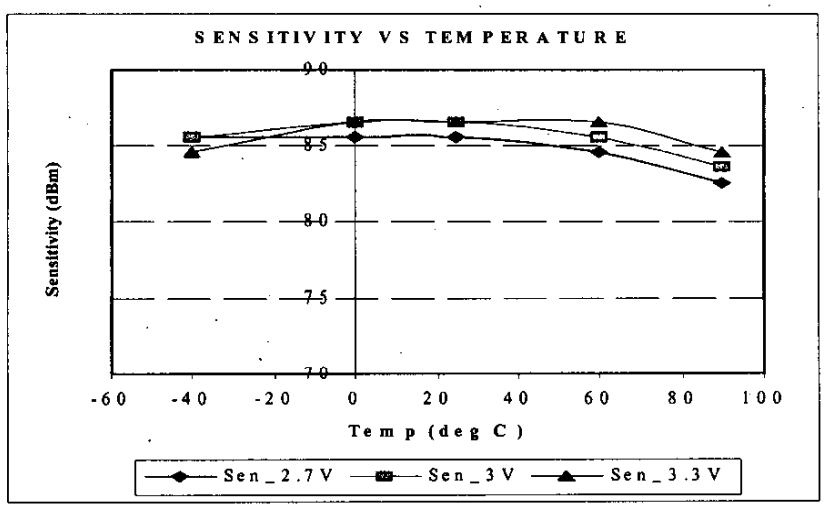

Fig. 5. Sensitivity Variation across Vdd and Temperature